Electrical Test: Surface Finish vs. Water Marks

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After a brief time off and a successful IPC APEX EXPO, I'm here to field your questions and get back to business. Thank you to all that stopped by to see me at the show. It was a good year in San Diego and the weather (as usual) mostly cooperated. Looks like we'll all be heading back to Vegas next year!

This month we will look at the ballet of sorts, performed by electrical test vs. surface finishes—namely witness marks. Over time, new finishes have come to market. Some allow better conductivity while others reduce overall cost of precious materials. Regardless of the finish, electrical test must be performed on these circuits. With that comes the caveat of how much of a witness mark can be left on any given landing pad and still be acceptable to the CM or the final OEM user.

First, we must understand what a witness mark actually is. In "down home" terms, when building a fence the old-fashioned way, you typically hammer the planks of the fence to the supporting framework. When the hammer hits the nail, the hammer leaves (unless you are really good) a round indentation into the board you are attaching, a.k.a. a witness mark! This is a mark indicating the historic process that was applied. Witness marks in electrical test are much the same. When an electrical test is performed, a physical contact is made from the machine to the PCB. This works the same whether it is from a translator fixture on a bed of nails or the direct contact from a flying probe. The combination of the surface finish being used and the type of electrical tester being used can produce a wide array of witness marks. Most of these marks are benign and acceptable, but in severe cases they can be destructive resulting in costly rework or even worse, scrap!

Some finishes are more critical than others. These range from HASL, immersion tin and ENIG, to the critical finishes such as immersion gold, immersion silver, soft gold and the ultimately delicate wire-bond. Customer requirements and industry specifications have guidelines regarding what acceptable witness marks may be. In the general specification for the manufacture of PWBs, the specification references the

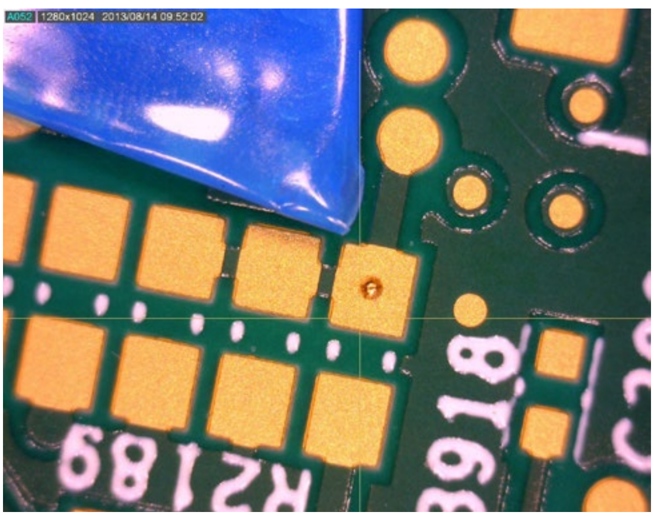

Figure 1: Pin damage.

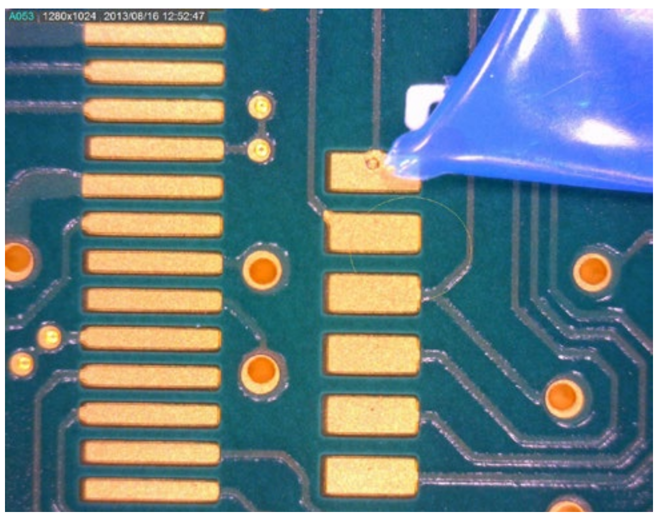

Figure 2: Pin damage.

ELECTRICAL TEST: SURFACE FINISH VS. WATER MARKS *continues*

"pristine area" of the landing pad when gauging the acceptability of the witness mark. For a rectangle SMT landing pad, the pristine area is defined by the central 80% of the land width x 80% of the land length. For round SMT landing pads, the pristine area is defined as the central 80% of the diameter. Electrical test probe witness marks within the pristine area for Class I, Class II and Class III are considered cosmetic in nature and are acceptable provided the requirements of the final finish are met (IPC-6012C).

As noted earlier, witness marks may be different depending on the type of test solution being used. Fixtures use either solid pins or spring pins with different options for head styles. These can be round (conical), spear point or even chisel point. The main goal for Electrical test is to perform the test required while minimizing the witness mark to the PCB. Many are under of the opinion that fixtures are the main source of pad damage resulting from electrical test and in many cases this is true. Due to the mechanics of the fixture, translator pins, stripper plates (cassettes) there are many factors in play that can cause a pin to "lock" and apply excessive pressure/force to the delicate landing pad. Figures 1 & 2 provide examples of what can result from excessive pressure applied to the PCB.

The above examples are typical of "pin lock" or the pin stuck when the fixture is compressed. In Figure 1 the damage is in the pristine area and is severe enough that copper is exposed. In most cases, this PCB is scrap due to the excessive pin hit unless reworked if allowed. In Figure 2, the hit is less severe and is just on the borderline of the pristine area. This pin hit is not exposing copper and in most cases will be allowed.

Flying probe machines are much more delicate when it comes to witness marks, but they are not totally immune either. Although they do provide a very light touch to the PCB, other factors can increase witness marks from a flying probe. Compression values, X/Y/Z velocities and accelerations all come in to play with flying probe equipment.

Figure 3 gives an example of a witness mark created from a flying probe where one of the above noted parameters may be slightly out of tolerance. Figure 4 shows the common witness mark left by a flying probe.

The most delicate of all is the test of wire-bond. In most cases the direct probing of wire-bond pads is not recommended, as there is no copper structure under the gold and the pads are extremely vulnerable to damage. Many times, no witness mark in the pristine area is allowed. Solutions to this vary from up-line on the trace outside of the pristine area, the first available pad in the net closest to the wire-bond termination or a 2-pass test solution where the shorts test is performed on a stronger test point within the net and the continuity test is performed by covering the wire-bond area with a conductive material, creating a special test program to check the wire-bond terminations to another point in their net to validate continuity. This

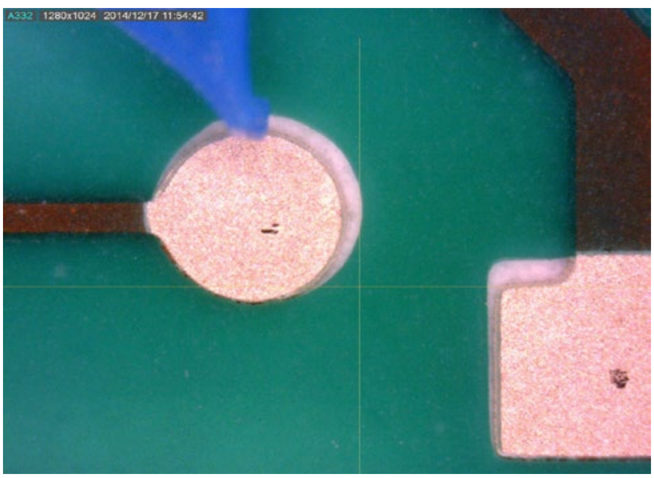

Figure 3: FP hard hit.

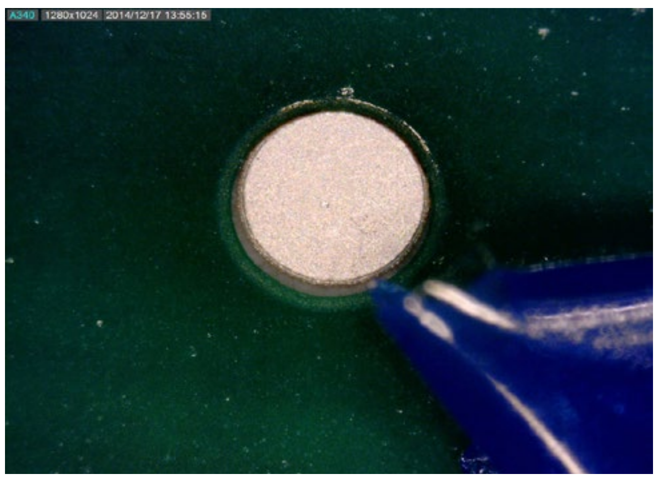

Figure 4: FP standard hit.

is a very safe way to minimize the possibility of damage to the wire-bond. Figure 5 shows how easily a wire-bond pad can be damaged.

Witness marks are inevitable during electrical test in some form or another. Surface finishes are also an important factor. In today's manufacturing arena, the older mindsets of "one setting fits all" for the electrical test machines cannot be used. In many cases the machines, both flying probe and grid test machines, may require adjustments depending on the surface finish. It may not be as critical for compression values when testing the harder finishes such as HASL but when testing the delicate finishes, extreme care must be exercised or costly and unnecessary rework may have to be done to the PCBs; in extreme cases, the PCB may have to be scrapped which causes delivery delays, rebuilds and unhappy customers!

See you next month and keep reading and Testing Todd! (Your questions are welcome!) **PCB**

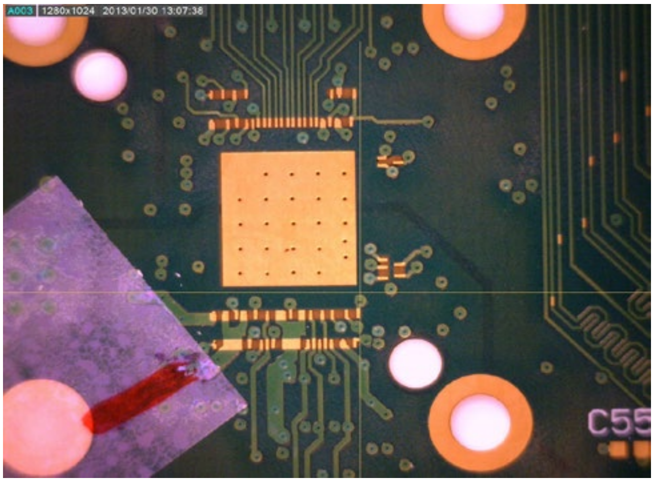

Figure 5: Wire-bond damage.

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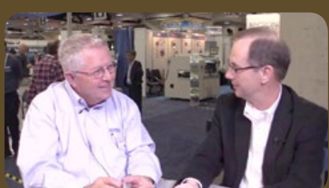

The HDP User Group engages in a variety of cooperative research projects that benefit the industry. I-Connect007 Guest Editor Dick Crowe speaks with Facilitator John Davignon, who explains the objectives of the Smooth Copper Signal Integrity project, and invites interested parties to participate

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