TESTING TODD

2015: It's a Wrap!

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With Thanksgiving in the U.S. a recent memory and many of us not on speaking terms with our bathroom scale, we now look forward to Christmas and the continuance and closure of the Holiday Season. With that comes the closure of 2015 and the new challenges of 2016. With my last column of the year I thought I would publish some of the highlight questions I received over the past year:

Q: My print says "Test to IPC-6012 Class 3/A." What is the difference between Class 3 and Class 3/A?

A: IPC Class 3 is standard commercial/military/medical/communication product where high reliability is demanded. Continuity thresholds are 10 ohms or less and isolation thresholds are 10M ohms or greater. A mandatory test voltage is not specified other than IPC-9252A requirements of either the test voltage specified on the print or procurement document, the rated voltage of the PCB as a minimum if stated on the print or 40 volts minimum if no other direction is given.

IPC Class 3/A is the IPC-6012 *Exception for Aerospace and Military Avionics*. When this requirement is specified the test voltage shall be 250 V minimum, the isolation resistance *shall be* 100 M ohms minimum and the continuity resistance shall be 10 ohms or less.

Q: What is adjacency testing?

A: Flying probe machines use what is called "adjacency testing" when performing isolation (shorts) testing. Unlike a fixture tester that tests all nets to one another during the test, the flying probes test only nets that are adjacent (next to each other). In most applications, the flying probe performs line-of-sight or horizontal adja-

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cency. This means that it is limited to the surface of the same layer. A single net is tested to all adjacent nets within the predetermined window. Industry standard for this window is .050" (1.27 mm.) The primary net is tested to all nets within that window. Nets outside that window to the primary net are disregarded.

The other type of adjacency is Z-axis, or vertical adjacency. In this method, not only are the line-of-sight nets checked to the adjacency window but also nets on the adjacent layers within the predefined Z-axis window. More fabrication information is required for programming Z-axis adjacency. The stack-up of the PCB must be calculated. Specific thicknesses of dielectrics and core materials are used to define the appropriate adjacency window. If not calculated correctly the window may be created too large and accidentally pick up a layer too far away and cause excess test time, or be calculated too small and not test as required.

Another hybrid feature in adjacency testing is the ability to create multiple adjacency windows on the same layer. This can be helpful if the PCB has a mix of tight trace/space coupled with other areas with larger spacing than the standard .050" window. One can define the .050" window for the areas of the product where the finer pitch/spacing indicates and then define a larger window for areas of the product outside the standard window but are at risk for possible discontinuity.

Q: My print says a dielectric withstanding test is required. It says to test to IPC-TM-650 Condition B. What is that?

A: In IPC-TM-650 (Test Methods) section 5.2.1 outlines the test conditions. There are two: Condition A and Condition B.

- Condition A: 500+15/-0 volts DC
- Condition B: 1000+25/-0 volts DC

In either case, there are two other variables considered, ramp and dwell.

Ramp = time in seconds from test start to reach full test voltage

Dwell = time in seconds to hold the test at test voltage.

Standards are 100V/sec ramp and 30 seconds dwell unless otherwise specified. (Note: If no condition is specified for the test, Condition A is the default.)

Q: We are testing a board that requires Class 3 electrical performance but we keep getting a few opens that will not pass at these parameters. What are my options?

A: This has become a rather common question. Class 3 product does require all nets to be 10 ohms or less. However you cannot bend the rules of mathematics. In most cases even large designs will pass under Class 3 parameters, however once a single net becomes too long with regard to length of the run from end point to end point, the math just doesn't work. That is why in Table 4-1 of IPC-9252A there is a note to compensate for this. For refereeing purposes the value of 0.5 ohms per .25 mm (.984") of circuit length shall apply. So if the circuit length is known, a calculation can be made for acceptance of that net even though it does not pass at the 10 ohm stated continuity requirement.

If a pass tag or pass requirement on the machine is mandatory, another solution is to program the net(s) as embedded components. The calculated resistance of the long nets can be programmed in the netlist to allow the rest of the board to be tested at 10 ohms. In the end you will receive your pass tag or green light from the machine.

Thank you all for reading this past year. Also, many thanks to Editors Lisa Lucke, Patty Goldman, and all the folks at PCB007 for being a great team to work with! Keep the questions and comments coming! Hope you all have a great rest of the Holiday Season and see you next year! **PCB**

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