Flying Probe Testing vs. IPC-9252B

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Flying probe testing is extremely popular in today's manufacturing theatres. The main factor is cost reduction in contrast to dedicated fixtures and fixture testing. However, there are some limitations in flying probe testing when gauged against industry specifications—specifically, the use of indirect vs direct testing in Test Level C. Table 4-1 of IPC-9252B outlines the methodologies allowed over the different Test Levels. This month we will be discussing Test Level C as this level raises the most questions regarding the use of direct versus indirect test methods when testing product in the Test Level C class. First, we need to define some terms used in flying probe testing.

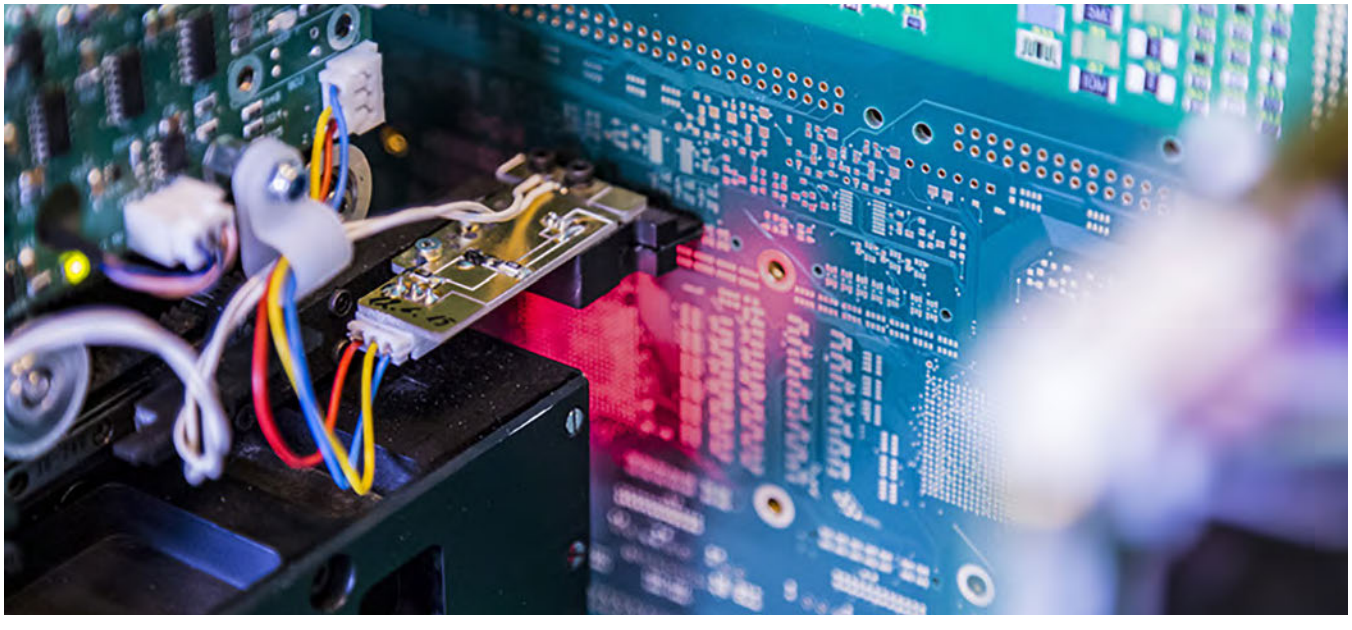
AABUS

The term AABUS, or "As Agreed Between User and Supplier," is used in IPC specifications where actions within a specific requirement are allowed, but require the mutual agreement between the user and manufacturer. This term is important as it amplifies the requirement for correct flow-down of customer requirements and any special allowances or deviation of the industry specifications. (See my April column regarding flow-down.)

Adjacency and Adjacency Window

The terms 'adjacency' and 'adjacency window' are used with flying probes defining the area for which the isolation test is performed. There are two types of adjacency: horizontal (line of sight) and vertical (Z-axis). As with fixture testers and parametric testing, the flying probes cannot accomplish a full parametric isolation test as they simply do not have the hardware. So the industry has accepted the practice of adjacency. How this works is that when a single net is interrogated for shorts it is tested against other nets in range or that are adjacent to that net. That range is defined as the adjacency window. The adjacency window is user-definable, however the specification IPC-9252B has recommended 0.050" (1.27 mm) as a default value for horizontal or line of sight adjacency.

When programming for vertical adjacency, there is more information required and the window is variable. One needs the stack-up in-



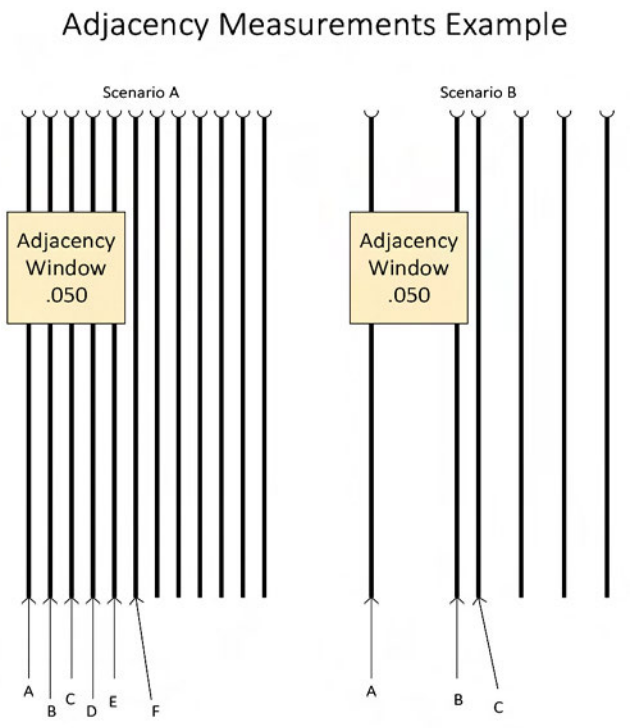


Figure 1: Adjacency windows.

formation as well as the core and foil thicknesses. If the vertical adjacency window is programmed too shallow, the risk of missing shorts to the adjacent later(s) is possible. If the window is too large you risk picking up too many layers and the test may become much longer than intended. It is necessary to remember that if the adjacency window is changed it can affect the time taken during for the isolation test to be performed. This is directly proportional to the window size. As the adjacency window increases the time to perform the test increases, as the Adjacency Window will possibly pick up more net "in range." Figure 1 illustrates how the window can affect the test based on the topography of the PCB using horizontal adjacency.

In Figure 1 we see two scenarios, scenario A and scenario B. When performing the isolation test this becomes important as the amount of measurements required during the test can be significantly different and affect time to perform the entire PCB test. In scenario A we see six different nets labeled A through F. We also see an adjacency window of .050". What we see here is when Net A is tested for shorts, it must be tested against nets B through E. This is four measurements. You will notice that Net F is not tested to Net A. Net F does not fall within range of the adjacency window.

Now in Figure 1 Scenario B, we have the same adjacency window but in this case, we have nets shown labeled A through C. When the isolation test is performed on net A there will be only one measurement. Net A will be only tested against Net B. Net C is again not within range or inside the adjacency window and therefore is not tested against Net A. So in Figure 1 you can see that PCB density can affect the amount of measurements required to perform the isolation test and thus affecting time required.

Direct Mode

Direct mode utilizes direct resistance measurements for all nets on the PCB. What this means is that during the continuity (opens) test all test points of the net are tested against the continuity threshold. Any net that violates the required resistance will be reported as a fault.

When the isolation test (shorts) is performed, each net is probed using the required voltage and isolation parameter. One must remember that when flying probes perform the isolation test they are performing it via an adjacency window as defined previously.

When direct mode is used, each PCB will take the same amount of time to test. This is because every net will be tested for continuity and isolation the same way each time. PCB 2 will take the same time as PCB 1 as well as PCB 3 and so on.

Indirect Mode

Indirect mode (also termed indirect testing by signature comparison or discharge testing) is the method where the flying probe develops speed over direct mode testing. In this method, the machine develops a capacitive master by gathering a capacitive signature of the board and then comparing subsequent boards to it. When the first PCB of an order is tested, the machine places a reference probe or probes down on the PCB reference plane or planes. It will then use the remaining probes to read a signature from all nets and record those finding to the master. Depending on the type of machine,

this may be direct capacitive measurements or capacitive "counts."

When the capacitive gather is complete on the first board it will perform a full direct mode test to validate the first board is actually conforming and does not have any defects. If no defects are found the capacitive master is written as "golden." If any defects are found, the master still will be written but the defective nets will be discounted from the master as they were nonconforming. When the second board is tested, the capacitive gather is done again. When it is complete the machine will compare the values from board number two to the master. If any of the readings are not within tolerance of the master, those nets will be placed in a retest file for direct mode probing. This could be for either possible opens or shorts. The amount of direct mode probing will be controlled by the anomalies found during the capacitive gather. The less discrepancies found against the master the less direct mode probing will be done. This is how the speed is gained during indirect testing.

Test Methods vs. IPC-9252B Test Level C

Now that we understand the two basic methods used in flying probe testing, what impact does this have on product in Performance Class 3? This can have a large effect based on whether indirect testing can be done or not. The 9252B specification does allow indirect testing for Performance Class 3 (Test Level C), but has the caveat of AABUS as defined previously. So as one reads the specification, if the allowance for indirect testing has not been stipulated in the flow-down, P.O., or customer specification, the default flying probe test method for Performance Class 3 (Test Level C) is direct mode.

How much of an impact can this be? It can be substantial based on the amount of test points, nets and adjacency pairs. We performed an experiment across five different PCBs with different amounts of test points, nets and adjacency pairs. In Table 1 we show the five different boards with their individual attributes.

Each of the PCBs 1–5 were tested in both direct mode and indirect mode. For our discussion, we will be doing a comparison based on the amount of measurements taken to test the individual boards. The reason we have used measurements instead of time required is that PCB topography is a variable and mechanical travel will not be the same nor can be correlated to test points. Measurements more directly show the contrasting between test methods.

For each of our PCBs in our experiment all went through direct mode test, indirect master generation, and nidirect subsequent board test.

In Table 2 we see how many measurements are taken for each type of test. As we discussed earlier, the amount of measurements required to perform direct mode test will not change. However, for indirect mode testing we see significant differences in the amount of measurements required. The indirect column is the amount of measurements required for subsequent boards prior to direct mode retest, as this can vary from board to board. What sticks out to us immediately is the advantage we see using Indirect testing vs. direct testing. In just our control group we

	Test Points	Nets	Adjacent Nets
PCB 1	5,865	1,762	18,840
PCB 2	5,677	1,671	17,517
PCB 3	4,291	1,325	12,433
PCB 4	10,871	2,440	24,451
PCB 5	28,728	7,088	69,053

Table 1: PCB group.

	Test Points	Indirect	Direct	Indirect to Direct
PCB 1	5,865	7,012	22,943	327%
PCB 2	5,677	6,753	21,523	319%
PCB 3	4,291	5,061	15,404	304%
PCB 4	10,871	12,515	32,882	263%
PCB 5	28,728	33,263	90,693	273%

Table 2: Indirect and direct test method measurements.

	Test Points	Indirect	Direct	Hybrid Test		Indirect to Direct	Hybrid to Direct
PCB 1	5,865	7,012	22,943	10,910		327%	210%
PCB 2	5,677	6,753	21,523	10,559		319%	204%
PCB 3	4,291	5,061	15,404	7,879		304%	196%
PCB 4	10,871	12,515	32,882	20,525		263%	160%
PCB 5	28,728	33,263	90,693	53,821		273%	169%

Table 3: Indirect, direct and hybrid test measurements.

saw 263–327% difference in required measurements. Even though we see significant advantages to use Indirect over direct mode if there is no AABUS or allowance via procurement document, customer specification or other means we are bound to IPC-9252B and direct mode.

Hybrid Indirect Mode

What if there was a way to incorporate some of both modes into a method where capacitive gather is done, direct mode continuity is done and finally the isolation test via adjacency is done based on the results of the capacitive master? Well there is! The main requirement of most Test Level C product is the continuity resistance. In the IPC-9252B standard this is 10 ohms. The argument has been that in indirect mode you do not necessarily test the net for 10 ohms unless it happened to be captured in the retest file during capacitance gather. However, with this hybrid test the capacitive gather is done as normal for indirect testing and the first board will receive the full direct mode validation as required. The change is how the second and subsequent boards are tested. They will receive the capacitive gather but this will only be used for retest during the isolation adjacency test. With the hybrid test all nets will be tested for continuity as in direct mode. For isolation, only nets that were found possibly faulty during the capacitive gather and placed in the retest file will be tested. This will reduce the amount of isolation tests required.

So how does this new mode compare against direct and indirect mode? In Table 3 we have added a column for hybrid test.

We see from Table 3 that we still have a reduction in measurements over our direct ode baseline. Of course, we did not expect the reduction as shown for indirect testing but the reduction to 160–210% is quite favorable. In fact, if we average our results from our control group, we see that 297% more measurements are required in direct vs. indirect testing. We also see that there is an average of 188% more measurements required in direct mode vs. hybrid test mode.

Conclusion

When flying probe testing under the requirements of Test Level C, we are bound by the default direct mode. We can see from our experiment that this could cause an average increase in measurements of 297% over indirect testing. However, without satisfying the AABUS requirement the extra measurements are required. And yes, this will take extra time. **PCB**

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