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Understanding the Fine Print

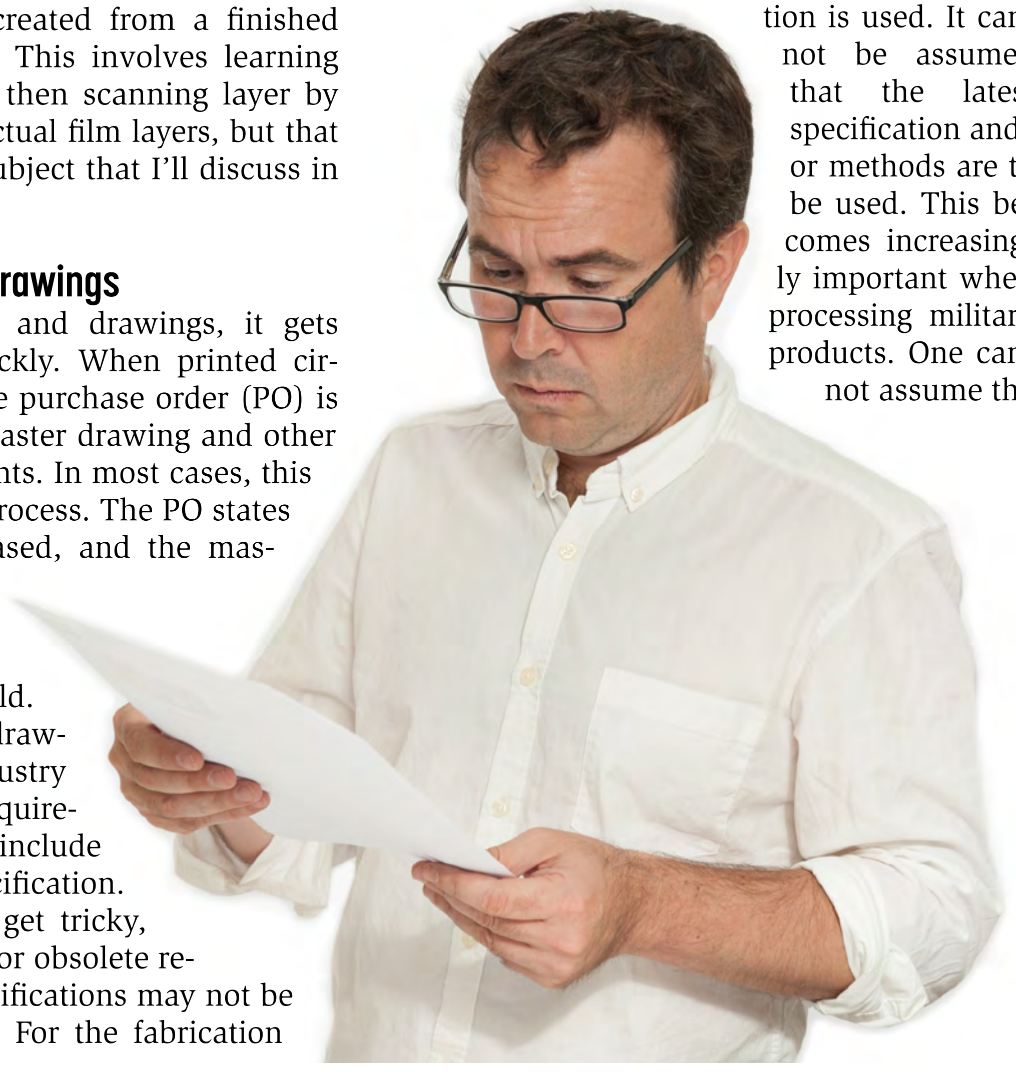
Testing Todd
Feature Column by Todd Kolmodin, GARDIEN SERVICES USA

New technologies are emerging each day with more stringent requirements than the past. Also, reversals in obsolescence programs bring products back to the market for which the original documentation and/or requirements are ancient compared to today's standards; in some cases, this documentation is even lost. Further, it is not uncommon to find that original artwork isn't available or that the part must be recreated from a finished circuit board sample. This involves learning a netlist profile and then scanning layer by layer to recreate the actual film layers, but that is a whole different subject that I'll discuss in a future column.

Specifications and Drawings

With specifications and drawings, it gets complicated very quickly. When printed circuits are procured, the purchase order (PO) is sent along with the master drawing and other deliverable requirements. In most cases, this is a straight forward process. The PO states what is being purchased, and the master drawing outlines the specifics and instructions on what is required for the build. Usually, the master drawing will specify industry specifications and requirements, which may include a special OEM specification. This is where it can get tricky, especially for historic or obsolete rebuilds. These old specifications may not be available. Now what? For the fabrication house, this often requires consulting with the OEM and either obtaining the lost document or acquiring a deviation or waiver for the lost document.

Even though the product may be a new build, there's a chance that the master drawing calls out for an older specification. Diligence is required by the fabrication house to make sure that the proper specification is used. It cannot be assumed that the latest specification and/or methods are to be used. This becomes increasingly important when processing military products. One cannot assume the



latest build specification is to be used. Older designs by OEM military contractors may call for older revisions of say MIL-PRF-31032, 55110, and 50884. For electrical test (ET), this can be especially significant.

Advances in test technology have brought new methodologies that were not allowed or even known in the older revisions of specifications. Just because the latest revision of a specification allows the use of these technologies, one cannot assume the new options apply. If an older specification is called, the requirements of that specification shall be used. This can be challenging for a third-party ET contractor.

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Many times, the ET contractor may have access to the master drawing only when the order is being processed. Job-specific notes may be added to the ET database for future reference, but special notes may be lost when the job returns to the fabrication house. This is where it is crucial to save the notes or retain a copy of the master drawing. Most ET contractors will have NDAs with their fabrication houses, so this isn't usually a problem. However, this becomes extremely important when the fabrication house or ET contractor is audited and allows absolute traceability and assurance that the product was built and tested as originally designed.

Certificate of Compliance Documents

This brings up another item that comes up quite frequently on the certificate of compliance (C of C) documents for ET. What specification should appear on the C of C for ET is a confusing topic. A master drawing may state, "Build to IPC-6012D." Should the ET C of C state IPC-6012D? The answer is no. If the C of C were to say IPC-6012D, it could be interpreted that the ET C of C is certifying the entire build, which it is not; it is only certifying the product was tested.

Reading the fine print in most build specifications will state that ET shall be in accordance with IPC-9252; that is the specific specification regarding ET of unpopulated printed wiring boards. The exception is when the aerospace and military avionics addendums are called from either 6012C or 6012DS. These require atypical test parameters outside of the standard 9252, and those specifications should appear on the C of C, in this case.

Military

Just because MIL-PRF-31032 is the current specification does not mean that it is automatic. Many military master drawings call out MIL-PRF-55110. MIL-PRF-55110 is alive and well, and if called, shall be used. But there is a vast inventory of military products out there that was designed long before the release of MIL-PRF-31032. Reorders of these products will require adherence to the older specification. Fabrication houses and ET contractors must be aware of this and adjust build and test methodologies to be compliant with the specification.

Another common issue is with MIL-PRF-31032 and the performance "slash sheets." An ET C of C is non-compliant if it just states MIL-PRF-32032. The Defense Logistics Agency (DLA) is very specific on this issue. A build to MIL-PRF-31032 must also state which applicable slash sheet the product was built to and also tested. This will be MIL-PRF-31032/1, /2, /3, /4, /5, or /6 with their appropriate revision and amendment level if applicable. The fine print here is that if the performance class (slash sheet) is not provided in the procurement and/or master drawing, this must be remedied before build and test. Failure to do so can (and will) result in a nonconformance during a DLA audit, so be forewarned.

Conclusion

Overall, you must read the fine print when viewing specifications and drawings. Just because the master drawing states an IPC general build specification does not mean an ET C of C will state that specification. Most IPC specification call for IPC-9252 as the ET specification, and it is correct that the ET C of C state IPC-9252 revision, class, and test level. The only exception is for aerospace and military avionics special requirements. It is also not uncommon to see the IPC-9252 specification on an ET C of C along with an applicable military specification. Many military specifications also call for testing to be in accordance with IPC-9252. However, certified test for military products must state the applicable performance specification used to be recorded for annual reporting and information retention. **PCB007**

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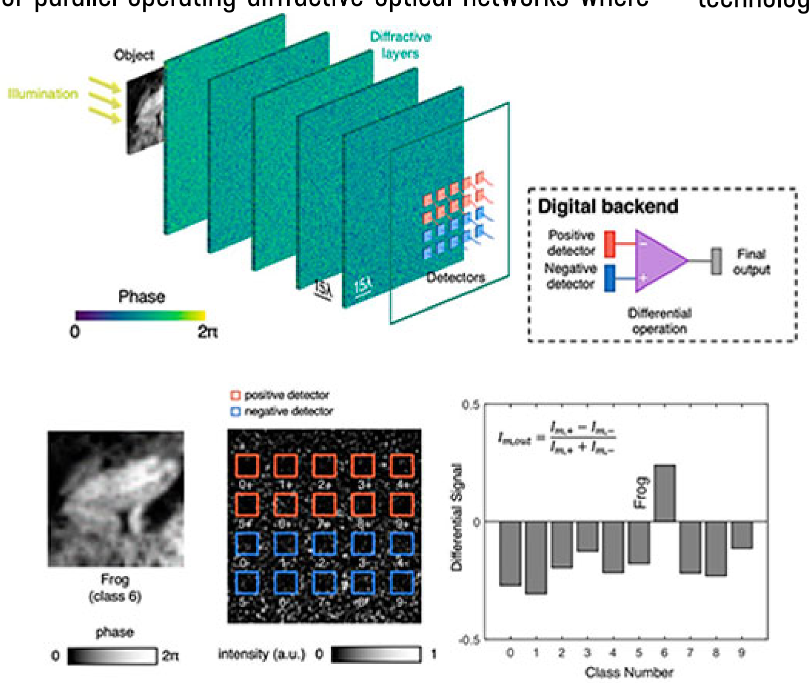
All-optical Diffractive Neural Network Closes Performance Gap With Electronic Neural Networks

A new paper in *Advanced Photonics,* an open-access journal co-published by SPIE, the international society for optics and photonics, and Chinese Laser Press (CLP), demonstrates distinct improvements to the inference and generalization performance of diffractive optical neural networks.

One of the key improvements discussed in the paper, "Class-specific differential detection in diffractive optical neural networks improves inference accuracy," incorporates a differential detection scheme combined with a set of parallel-operating diffractive optical networks where each individual network of this set is specialized to specifically recognize a sub-group of object classes.

According to SPIE Fellow Aydogan Ozcan of the University of California, Los Angeles, and one of the paper's authors, these results "provide a major advancement to bring optical neural network-based low-power and low-latency solutions for various machine-learning applications."

This latest research is a significant advance to Ozcan's optical machine-learning framework. The finessing of this technology is especially significant for recognizing target objects more quickly and with significantly less power than standard computer-based machine learning systems. Ultimately, it may provide major advantages for autonomous vehicles, robotics, and various defense-related applications, among others.



These latest systematic advances in diffractive optical network designs, in particular, have the potential to advance the development of next-generation, task-specific, and intelligent computational camera systems. The article authors are Jingxi Li, Deniz Mengu, Yi Luo, Yair Rivenson, and Aydogan Ozcan of the University of California at Los Angeles Department of Electrical and Computer Engineering and California NanoSystems Institute in Los Angeles, California, USA. (Source: SPIE)